

## TC551001APL/AFL/AFTL/ATRL-70/85/10(LT)

### SILICON GATE CMOS

### 131,072 WORD x 8 BIT STATIC RAM

#### Description

The TC551001APL is a 1,048,576 bit CMOS static random access memory organized as 131,072 words by 8 bits and operated from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (typ.) and a minimum cycle time of 70ns. When  $\overline{CE1}$  is a logical high, or CE2 is low, the device is placed in a low power standby mode in which the standby current is 2 $\mu$ A typically. The TC551001APL has three control inputs. Chip enable inputs ( $\overline{CE1}$ , CE2) allow for device selection and data retention control, while an output enable input ( $\overline{OE}$ ) provides fast memory access. The TC551001APL is suitable for use in microprocessor systems where high speed, low power, and battery backup are required. The TC551001APL-(LT) has an operating temperature range of -20 ~ 70°C so it is suitable for use in low temperature applications.

The TC551001APL is offered in a standard dual-in-line 32-pin plastic package, a small outline plastic package, and a thin small outline plastic package (forward type, reverse type).

#### Features

- Low power dissipation: 27.5mW/MHz (typ.)
- Standby current: 100 $\mu$ A (max.)
- Single 5V power supply
- Access time (max.)

	TC551001APL/AFL/AFTL/ATRL		
	-70(LT)	-85(LT)	-10(LT)
Access Time	70ns	85ns	100ns
$\overline{CE1}$ Access Time	70ns	85ns	100ns
CE2 Access Time	70ns	85ns	100ns
$\overline{OE}$ Access Time	35ns	45ns	50ns

- Power down feature:  $\overline{CE1}$ , CE2
- Data retention supply voltage: 2.0 ~ 5.5V
- Wide operating temperature: -20 ~ 70°C
- Inputs and outputs TTL compatible
- Package
  - TC551001APL : DIP32-P-600
  - TC551001AFL : SOP32-P-525
  - TC551001AFTL : TSOP32-P-0820
  - TC551001ATRL : TSOP32-P-0820A

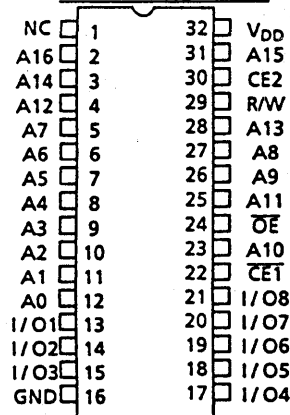
#### Pin Names

A0 ~ A16	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE1}$ , CE2	Chip Enable Inputs
I/O1 ~ I/O8	Data Input/Output
V <sub>DD</sub>	Power (+5V)
GND	Ground
NC	No Connection

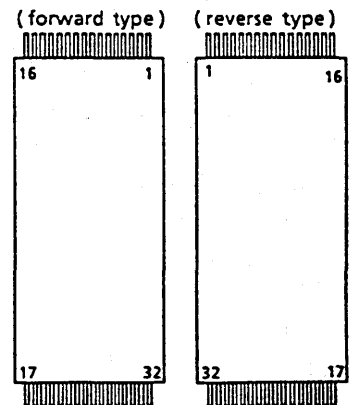
PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
PIN NAME	A <sub>11</sub>	A <sub>9</sub>	A <sub>8</sub>	A <sub>13</sub>	R/W	CE2	A <sub>15</sub>	V <sub>DD</sub>	NC	A <sub>16</sub>	A <sub>14</sub>	A <sub>12</sub>	A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>
PIN NO.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
PIN NAME	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE1}$	A <sub>10</sub>	$\overline{OE}$

#### Pin Connection (Top View)

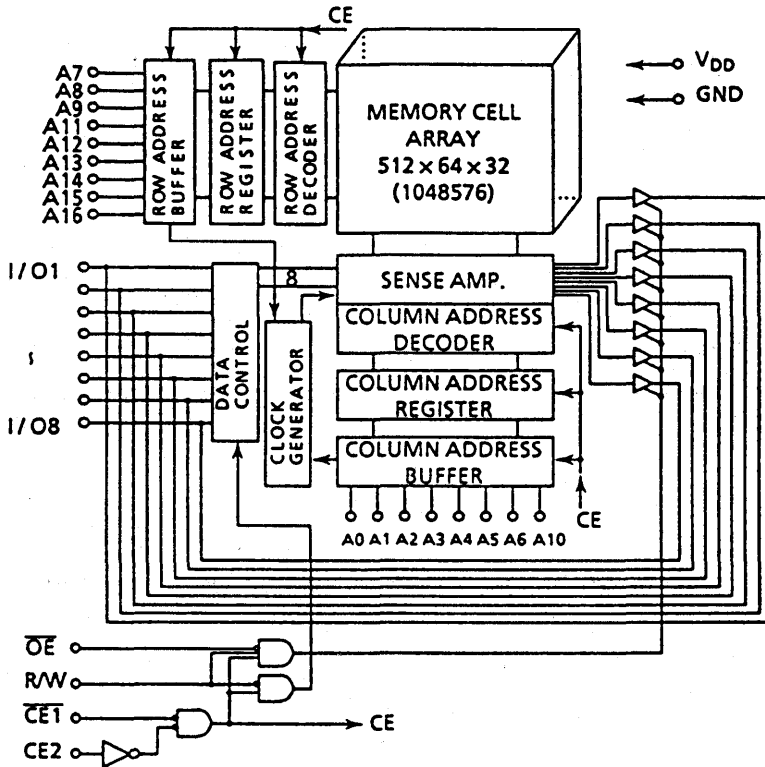
##### ○ 32 PIN DIP & SOP



##### ○ 32 PIN TSOP



Block Diagram



Operating Mode

MODE \ PIN	$\overline{CE1}$	CE2	$\overline{OE}$	R/W	I/O1 ~ I/O8	POWER
Read	L	H	L	H	D <sub>OUT</sub>	I <sub>DDO</sub>
Write	L	H	*	L	D <sub>IN</sub>	I <sub>DDO</sub>
Output Deselect	L	H	H	H	High-Z	I <sub>DDO</sub>
Standby	H	*	*	*	High-Z	I <sub>DDS</sub>
	*	L	*	*	High-Z	I <sub>DDS</sub>

\* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V <sub>DD</sub>	Power Supply Voltage	-0.3 ~ 7.0	V
V <sub>IN</sub>	Input Voltage	-0.3* ~ 7.0	V
V <sub>I/O</sub>	Input and Output Voltage	-0.5 ~ V <sub>DD</sub> + 0.5	V
P <sub>D</sub>	Power Dissipation	1.0/0.6**	W
T <sub>SOLDER</sub>	Soldering Temperature • Time	260 • 10	°C • sec
T <sub>STRG</sub>	Storage Temperature	-55 ~ 150	°C
T <sub>OPR</sub>	Operating Temperature	-20 ~ 70	°C

\* -3.0V with a pulse width of 50ns

\*\* SOP

## DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{DD}$	Power Supply Voltage	4.5	5.0	5.5	V
$V_{IH}$	Input High Voltage	2.4	–	$V_{DD} + 0.3$	
$V_{IL}$	Input Low Voltage	-0.3	–	0.6	
$V_{DH}$	Data Retention Supply Voltage	2.0	–	5.5	

DC Characteristics ( $T_a = -20 \sim 70^\circ\text{C}$ ,  $V_{DD} = 5V \pm 10\%$ )

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT		
$I_{LI}$	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	–	–	$\pm 1.0$	$\mu\text{A}$		
$I_{LO}$	Output Leakage Current	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ or $R/W = V_{IL}$ or $\overline{OE} = V_{IH}$ , $V_{OUT} = 0 \sim V_{DD}$	–	–	$\pm 1.0$	$\mu\text{A}$		
$I_{OH}$	Output High Current	$V_{OH} = 2.4\text{V}$	-1.0	–	–	mA		
$I_{OL}$	Output Low Current	$V_{OL} = 0.4\text{V}$	4.0	–	–	mA		
$I_{DDO1}$	Operating Current	$\overline{CE1} = V_{IL}$ and $CE2 = V_{IH}$ and $R/W = V_{IH}$ , $I_{OUT} = 0\text{mA}$ Other Inputs = $V_{IH}/V_{IL}$	$t_{\text{cycle}}$	Min.	–	–	70	mA
				1 $\mu\text{s}$	–	–	20	
$I_{DDO2}$		$\overline{CE1} = 0.2\text{V}$ and $CE2 = V_{DD} - 0.2\text{V}$ $R/W = V_{DD} - 0.2\text{V}$ $I_{OUT} = 0\text{mA}$ Other Inputs $= V_{DD} - 0.2\text{V}/0.2\text{V}$	$t_{\text{cycle}}$	Min.	–	–	60	
				1 $\mu\text{s}$	–	–	10	
$I_{DDS1}$	Standby Current	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$		–	–	–	3	mA
$I_{DDS2}^{(1)}$		$\overline{CE1} = V_{DD} - 0.2\text{V}$ or $CE2 = 0.2\text{V}$ $V_{DD} = 2.0\text{V} \sim 5.5\text{V}$	$T_a = -20 \sim 70^\circ\text{C}$	–	–	–	100	$\mu\text{A}$
		$T_a = 25^\circ\text{C}$	–	2	–	–		

Note (1): If  $\overline{CE1} \geq V_{DD} - 0.2\text{V}$ , the specified limits are guaranteed under the condition  $CE2 \geq V_{DD} - 0.2\text{V}$  or  $CE2 \leq 0.2\text{V}$ .

Capacitance\* ( $T_a = 25^\circ\text{C}$ ,  $f = 1\text{MHz}$ )

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
$C_{IN}$	Input Capacitance	$V_{IN} = \text{GND}$	10	$\text{pF}$
$C_{OUT}$	Output Capacitance	$V_{OUT} = \text{GND}$	10	

\*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = -20 ~ 70°C, V<sub>DD</sub> = 5V±10%)

## Read Cycle

SYMBOL	PARAMETER	TC551001APL/AFL/AFTL/ATRL						UNIT
		-70(LT)		-85(LT)		-10(LT)		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>RC</sub>	Read Cycle Time	70	–	85	–	100	–	ns
t <sub>ACC</sub>	Address Access Time	–	70	–	85	–	100	
t <sub>CO1</sub>	$\overline{CE1}$ Access Time	–	70	–	85	–	100	
t <sub>CO2</sub>	CE2 Access Time	–	70	–	85	–	100	
t <sub>OE</sub>	Output Enable to Output in Valid	–	35	–	45	–	50	
t <sub>COE</sub>	Chip Enable ( $\overline{CE1}$ , CE2) to Output in Low-Z	5	–	5	–	5	–	
t <sub>OEE</sub>	Output Enable to Output in Low-Z	0	–	0	–	0	–	
t <sub>OD</sub>	Chip Enable ( $\overline{CE1}$ , CE2) to Output in High-Z	–	25	–	30	–	35	
t <sub>ODO</sub>	Output Enable to Output in High-Z	–	25	–	30	–	35	
t <sub>OH</sub>	Output Data Hold Time	10	–	10	–	10	–	

## Write Cycle

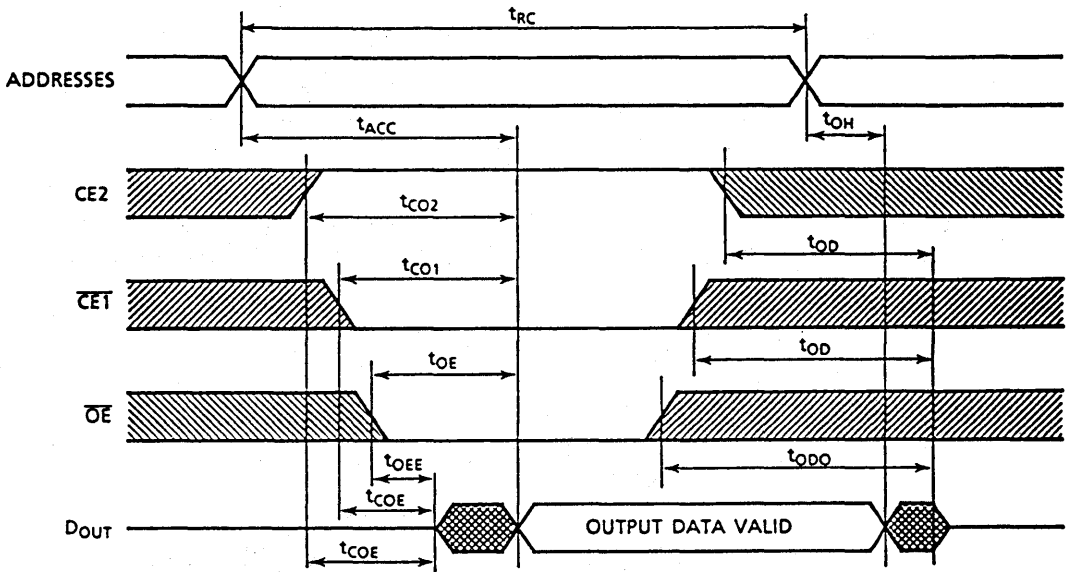
SYMBOL	PARAMETER	TC551001APL/AFL/AFTL/ATRL						UNIT
		-70(LT)		-85(LT)		-10(LT)		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>WC</sub>	Write Cycle Time	70	–	85	–	100	–	ns
t <sub>WP</sub>	Write Pulse Width	50	–	60	–	60	–	
t <sub>CW</sub>	Chip Selection to End of Write	60	–	75	–	80	–	
t <sub>AS</sub>	Address Setup Time	0	–	0	–	0	–	
t <sub>WR</sub>	Write Recovery Time	0	–	0	–	0	–	
t <sub>ODW</sub>	R/W to Output in High-Z	–	25	–	30	–	35	
t <sub>OEW</sub>	R/W to Output in Low-Z	0	–	0	–	0	–	
t <sub>DS</sub>	Data Setup Time	30	–	35	–	40	–	
t <sub>DH</sub>	Data Hold Time	0	–	0	–	0	–	

## AC Test Conditions

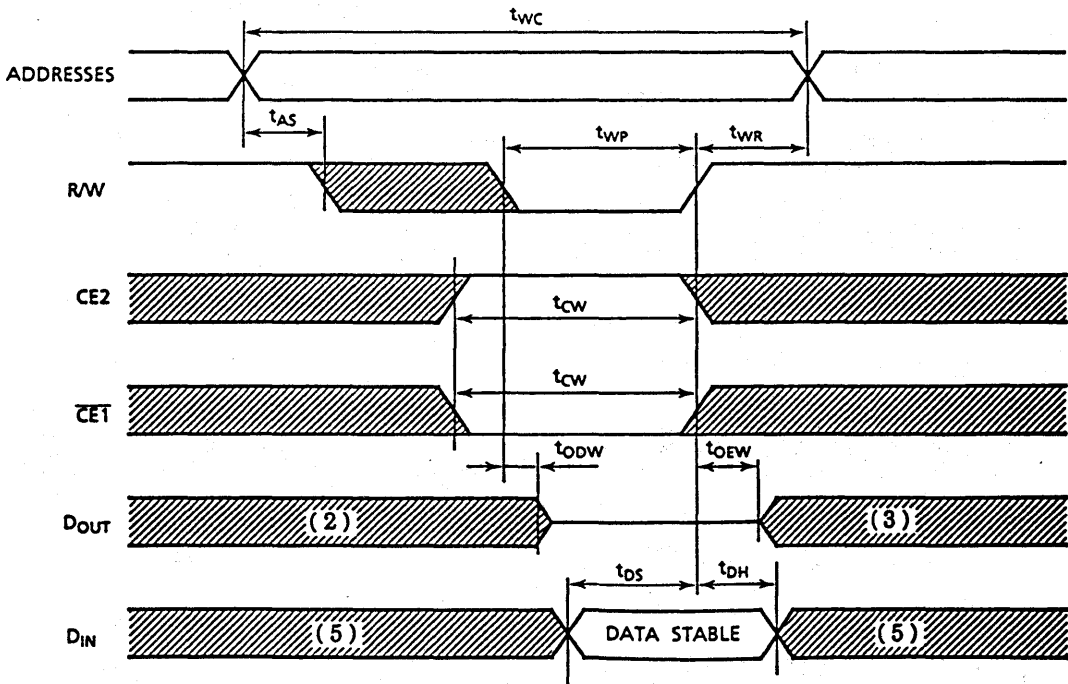
Input Pulse Levels	2.6V/0.4V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	1 TTL Gate and C <sub>L</sub> = 100pF

Timing Waveforms

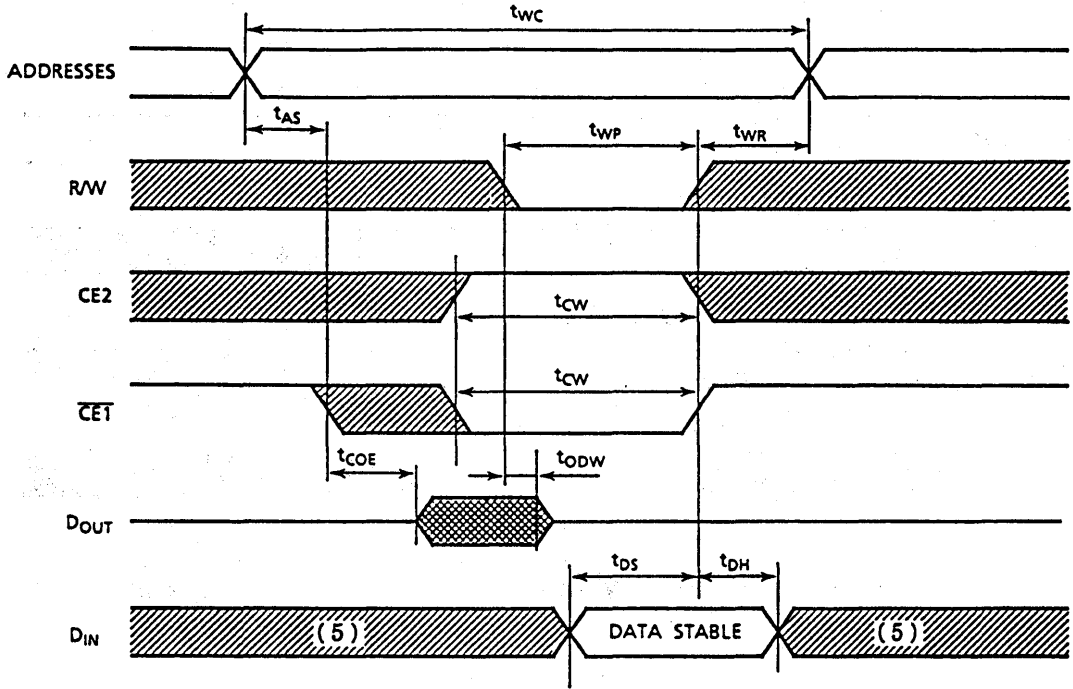
Read Cycle <sup>(1)</sup>



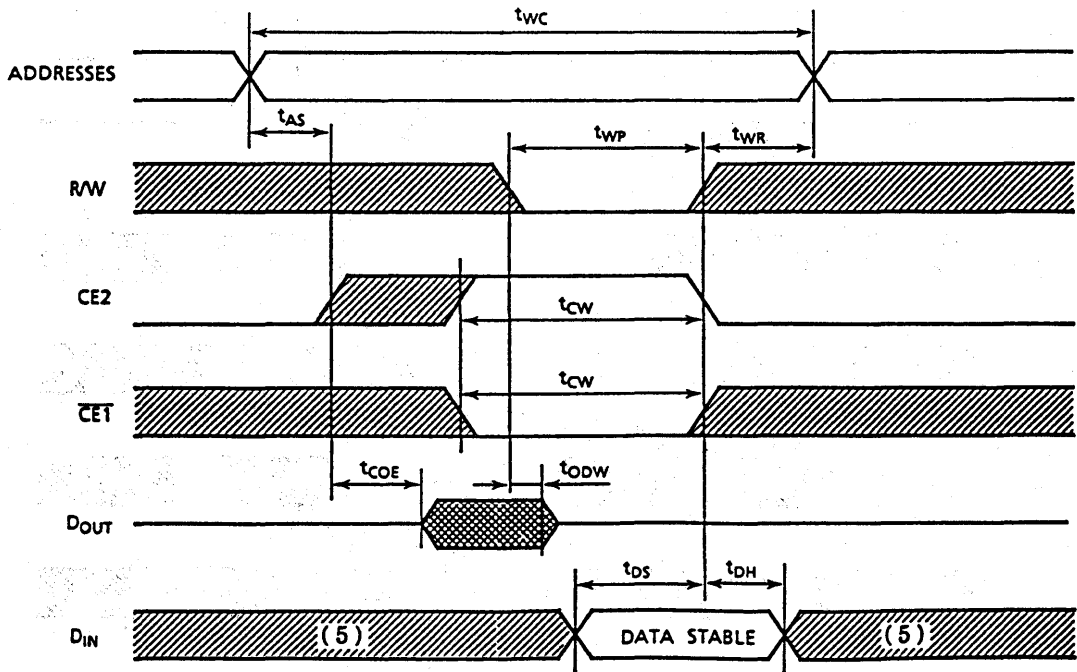
Write Cycle 1 <sup>(4)</sup> (R/W Controlled Write)



Write Cycle 2 <sup>(4)</sup> ( $\overline{\text{CE1}}$  Controlled Write)



Write Cycle 3 <sup>(4)</sup> (CE2 Controlled Write)



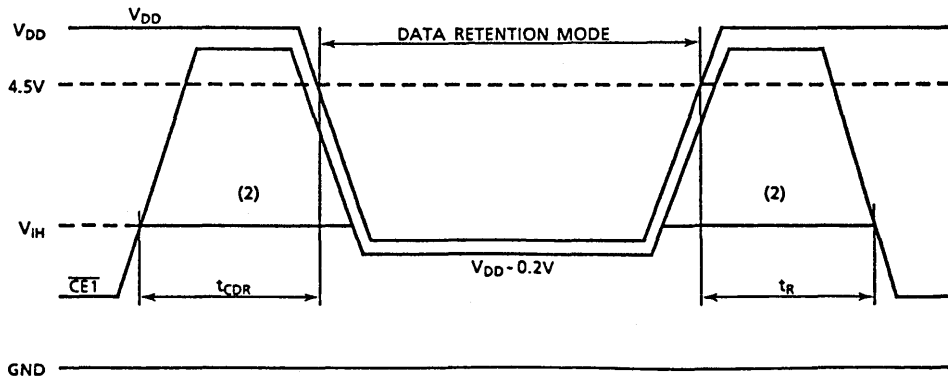
## Notes:

1. R/W is high for read cycles.
2. If the  $\overline{CE1}$  low transition or CE2 high transition occurs coincident with or after the R/W low transition, outputs remain in a high impedance state.
3. If the  $\overline{CE1}$  high transition or CE2 low transition occurs coincident with or prior to the R/W high transition, outputs remain in a high impedance state.
4. If  $\overline{OE}$  is high during a write cycle, the outputs are in a high impedance state during this period.
5. The I/O may be in the output state during this time; therefore input signals of opposite phase must not be applied.

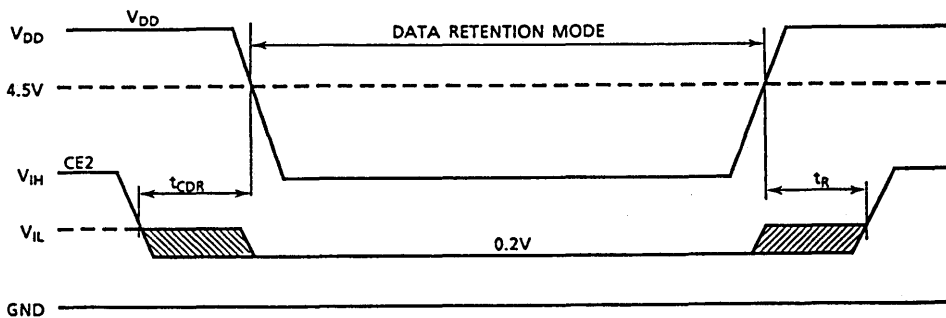
Data Retention Characteristics (Ta = -20 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	
V <sub>DH</sub>	Data Retention Supply Voltage	2.0	-	5.5	V	
I <sub>DDS2</sub>	Standby Current	V <sub>DH</sub> = 3.0V	-	-	50	μA
		V <sub>DH</sub> = 5.5V	-	-	100	
t <sub>CDR</sub>	Chip Deselect to Data Retention Mode	0	-	-	ns	
t <sub>R</sub>	Recovery Time	5	-	-	ms	

$\overline{CE1}$  Controlled Data Retention Mode (1)



CE2 Controlled Data Retention Mode (3)



Notes:

1. In the  $\overline{CE1}$  controlled data retention mode, minimum standby current is achieved under the condition  $CE2 \leq 0.2V$  or  $CE2 \geq V_{DD} - 0.2V$ .
2. If the  $V_{IH}$  of  $\overline{CE1}$  is 2.4V in operation, during the period that the  $V_{DD}$  voltage is going down from 4.5V to 2.6V,  $I_{DDS1}$  current flows.
3. In the CE2 controlled data retention mode, minimum standby current is achieved under the condition  $CE2 \leq 0.2V$ .