Philips Semiconductors-Signetics

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Status	Product Specification
FAST Products	

FAST 74F756, 74F757, 74F760 Buffers

74F756 Octal Inverter Buffer (Open Collector)
74F757 Octal Buffer (Open Collector)
74F760 Octal Buffer (Open Collector)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F756	9.0ns	40mA
74F757	9.0ns	45mA
74F760	9.0ns	45mA

FEATURES

- **Octal bus interface**
- **Open collector versions of 74F240, 74F241 and 74F244**

DESCRIPTION

The 74F756, 74F757 and 74F760 are octal buffers that are ideal for driving bus lines of buffer memory address registers. The 74F756 is the open collector version of 74F240, 74F757 is the open collector version of 74F241 and 74F760 is the open collector version of 74F244. These devices feature two Output Enables, $\overline{OE}_a$ and $\overline{OE}_b$ (or OE_b for the 'F757), each controlling four of the outputs.

ORDERING INFORMATION

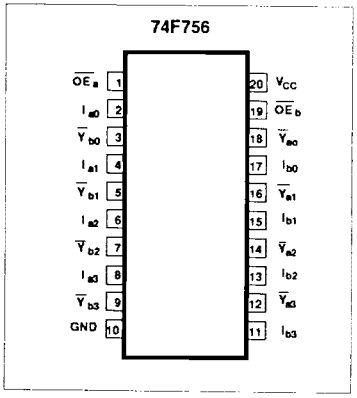
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F756N, N74F757N, N74F760N
20-Pin Plastic SOL	N74F756D, N74F757D, N74F760D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

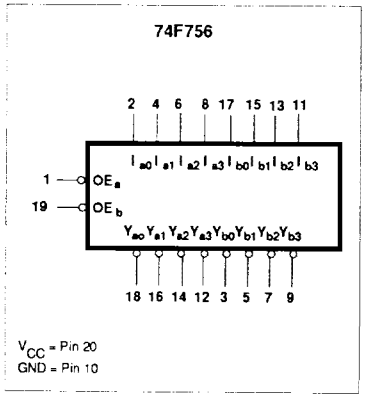
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{an}, I_{bn}	Data inputs	1.0/1.67	20μA/1.0mA
$\overline{OE}_a$ $\overline{OE}_b$	Output enable input (active Low)	1.0/1.67	20μA/1.0mA
OE_b	Output enable input (active High 'F757)	1.0/1.67	20μA/1.0mA
Y_{an}, Y_{bn}	Data outputs ('F757, 'F760)	OC/106.7	OC/64mA
$\overline{Y}_{an}$, $\overline{Y}_{bn}$	Data outputs ('F756)	OC/106.7	OC/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
OC= Open Collector

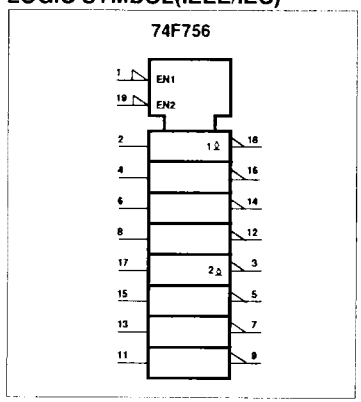
PIN CONFIGURATION



LOGIC SYMBOL

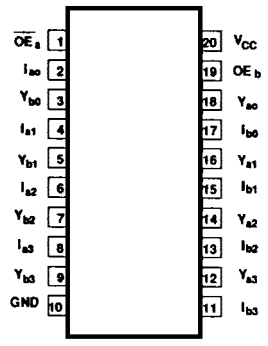


LOGIC SYMBOL(IEEE/IEC)



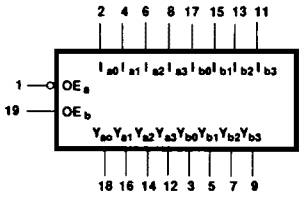
PIN CONFIGURATION

74F757



LOGIC SYMBOL

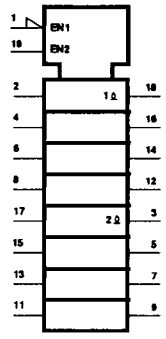
74F757



V_{CC} = Pin 20
GND = Pin 10

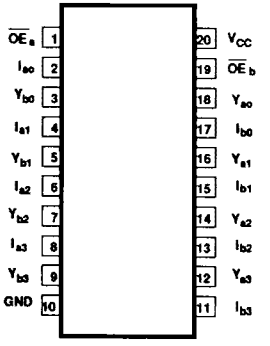
LOGIC SYMBOL(IEEE/IEC)

74F757



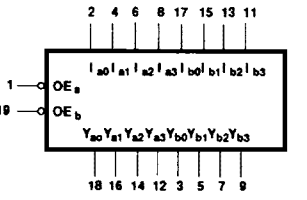
PIN CONFIGURATION

74F760



LOGIC SYMBOL

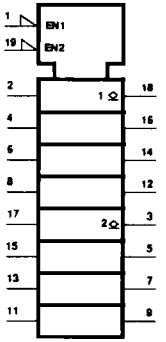
74F760



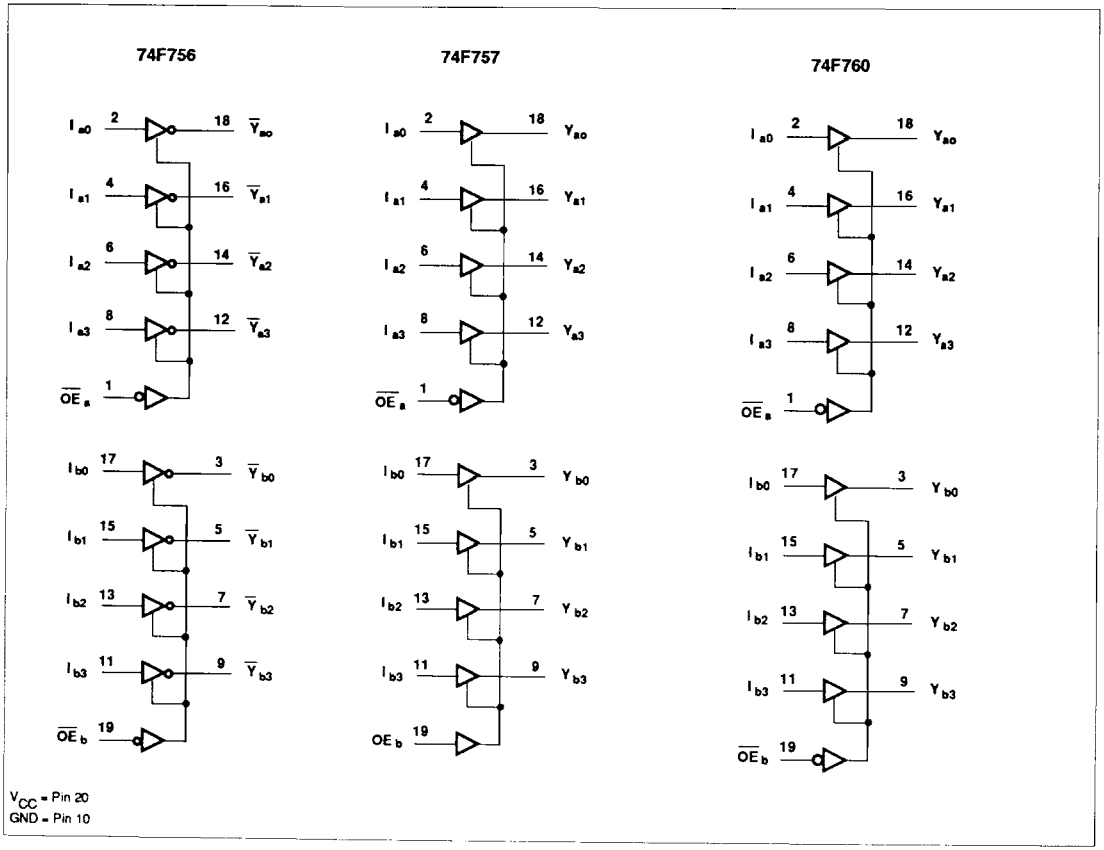
V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL(IEEE/IEC)

74F760



LOGIC DIAGRAM



FUNCTION TABLE, 74F756

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	$\overline{Y}_a$	$\overline{Y}_b$
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	H(off)	H(off)

FUNCTION TABLE, 74F760

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	Y_a	Y_b
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	H(off)	H(off)

FUNCTION TABLE, 74F757

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	OE_b	I_b	Y_a	Y_b
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	H(off)	H(off)

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER				UNIT
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_K	Input clamp current			-18	mA
V_{OH}	High level output voltage			4.5	V
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

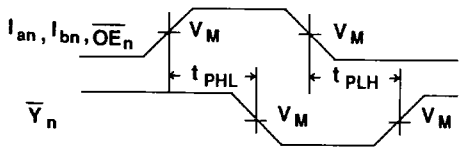
SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS			UNIT
							Min	Typ[2]	Max	
I_{OH}	High-level output current			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH}=MAX					250	µA
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OL}=48mA	±10%V_{CC}		0.38	0.55	V
					I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V					-1.0	mA
I_{CC}	Supply current (total)	74F756	I_{CCH}	V_{CC} = MAX				20	30	mA
			I_{CCL}					50	70	mA
		74F757	I_{CCH}					30	40	mA
			I_{CCL}					55	80	mA
		74F760	I_{CCH}					25	37	mA
			I_{CCL}					55	80	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

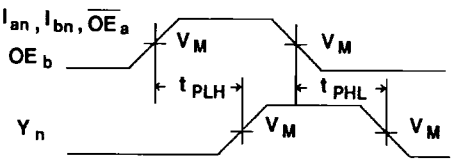
AC ELECTRICAL CHARACTERISITICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_{an}, I_{bn} to $\overline{Y}_n$	74F756	Waveform 1, 2	8.5 1.0	11.0 3.0	14.0 6.0	8.5 1.0	15.0 6.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}_n$ to $\overline{Y}_n$		Waveform 1, 2	9.0 5.0	11.5 7.0	14.5 10.0	9.0 4.5	15.0 10.5	ns
t_{PLH} t_{PHL}	Propagation delay I_{an}, I_{bn} to Y_n	74F757	Waveform 1, 2	7.5 3.0	10.5 5.5	13.5 8.5	7.5 3.0	14.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}_a$ or OE_b to Y_n		Waveform 1, 2	9.0 4.5	10.5 7.0	15.0 10.0	8.5 4.0	16.0 10.5	ns
t_{PLH} t_{PHL}	Propagation delay I_{an}, I_{bn} to Y_n	74F760	Waveform 1, 2	7.5 3.5	10.0 5.5	13.5 8.5	7.5 3.0	14.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}_n$ to Y_n		Waveform 1, 2	9.5 5.0	11.5 7.0	14.5 10.0	9.0 4.5	15.0 10.5	ns

AC WAVEFORMS



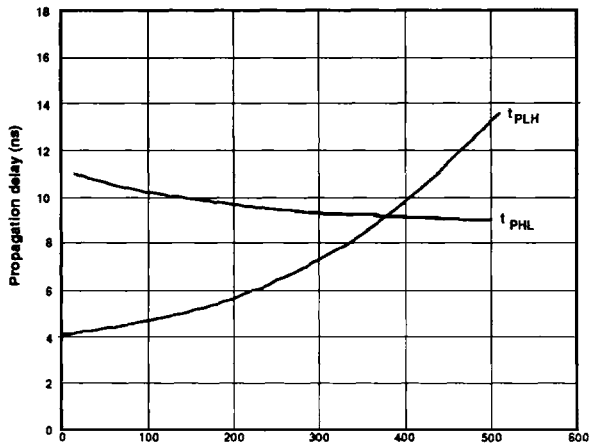
Waveform 1. For Inverting Outputs



Waveform 2. For Non-Inverting Outputs

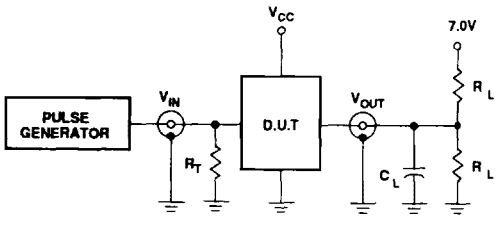
NOTE: For all waveforms, V_M = 1.5V.

TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS

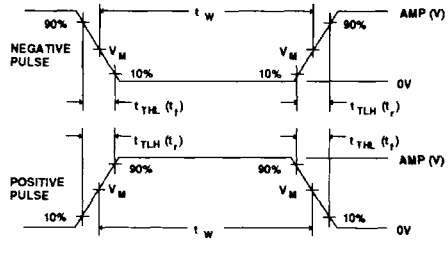


NOTE:
When using open-collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLH}. For example, changing the pull-up resistor value from 500 Ω to 100Ω will improve the t_{PLH} up to 50% with only slight increase in the t_{PHL}. However, if the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_{IL}'s of the receivers do not exceed the I_{OL} maximum specification.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Open Collector Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns